FIG. 1

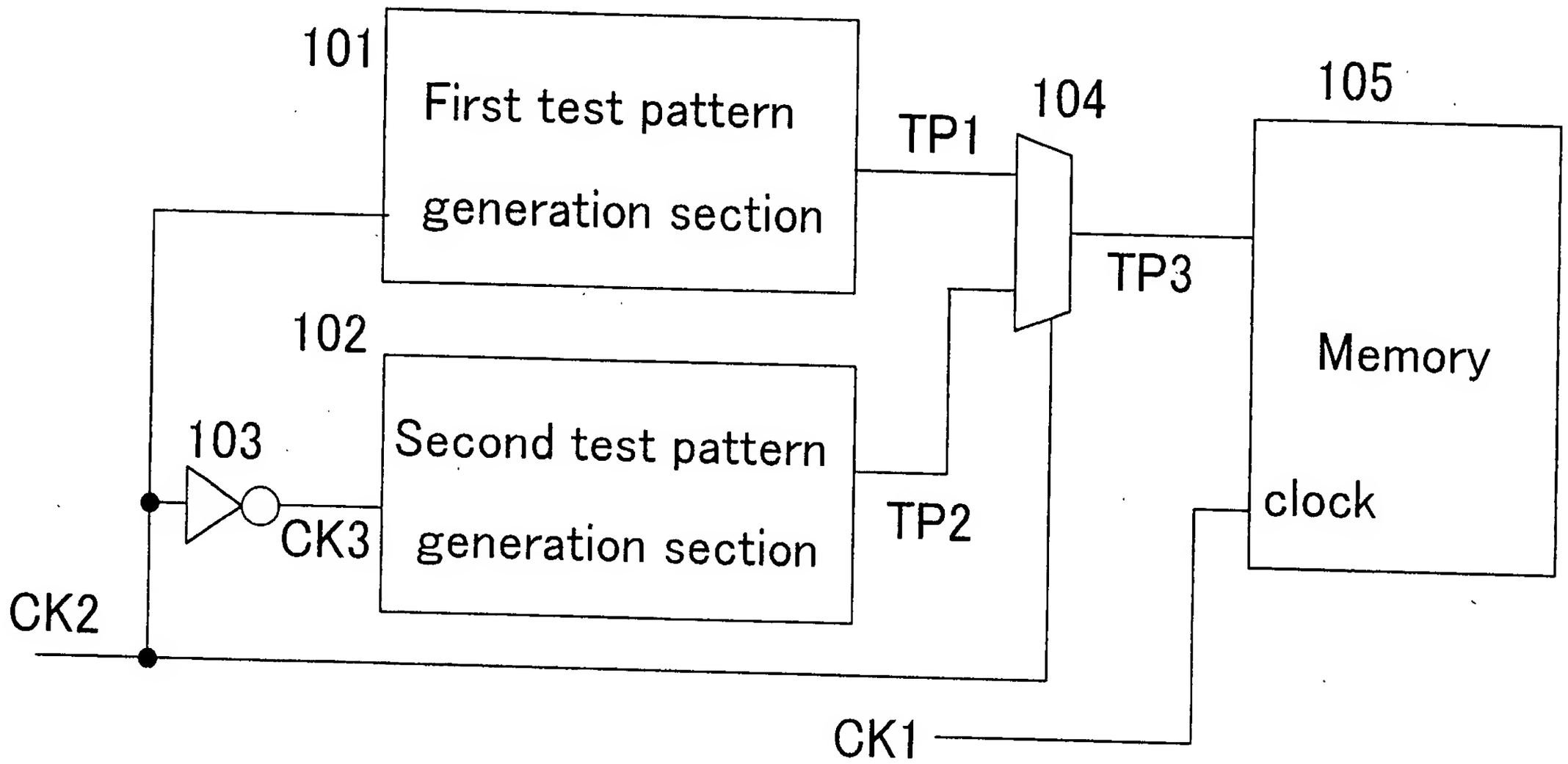

101
First test pattern generation section
TP1
104
105
TP3
Memory
clock
102
103
Second test pattern generation section
CK3
TP2
CK2
CK1

FIG. 2

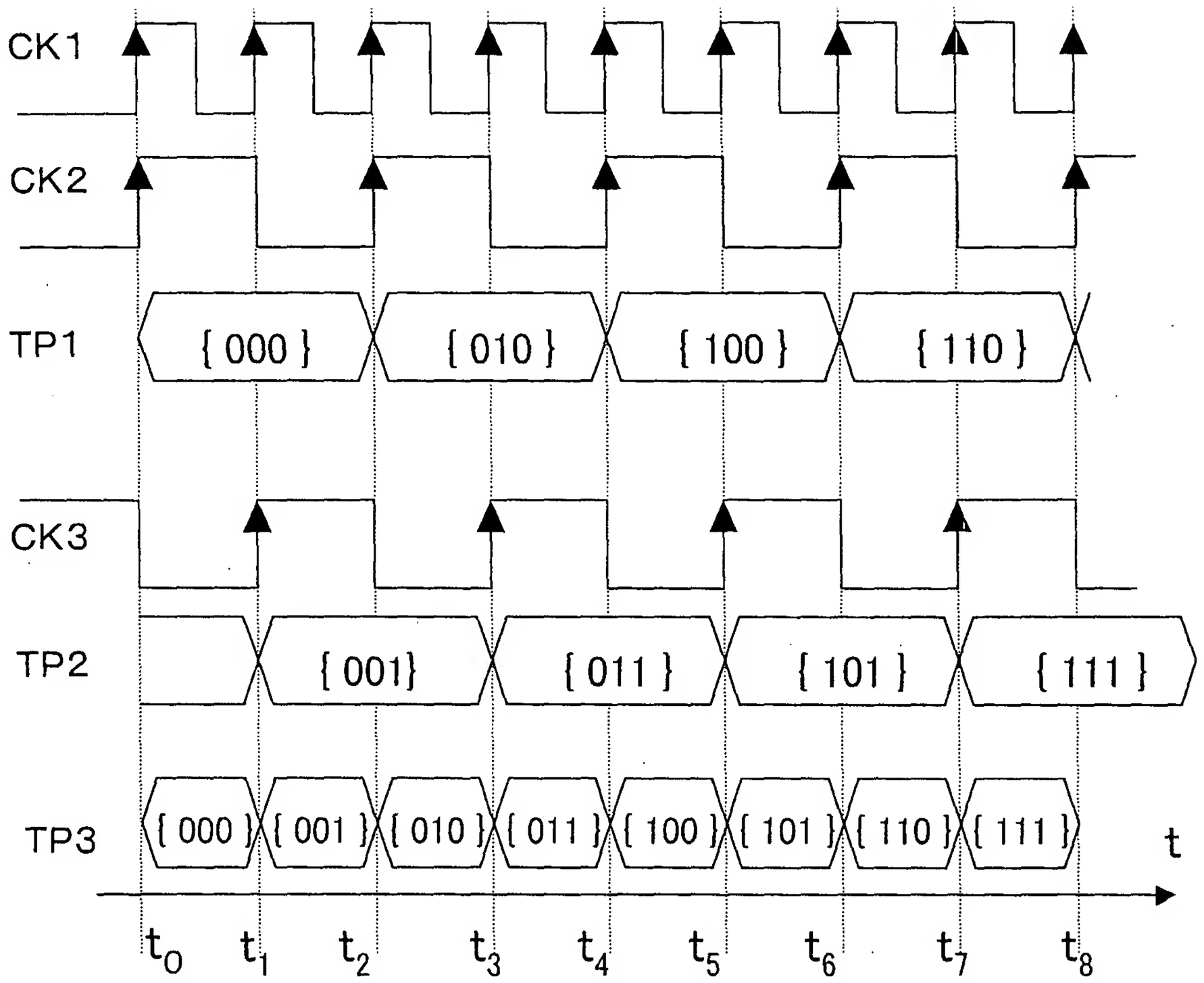

CK1
CK2
TP1
{ 000 }
{ 010 }
{ 100 }
{ 110 }
CK3
TP2
{ 001}
{ 011 }
{ 101 }
{ 111 }
TP3
{ 000 }
{ 001 }
{ 010 }
{ 011 }
{ 100 }
{ 101 }
{ 110 }
{ 111 }
t
t_0 t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8

FIG. 3

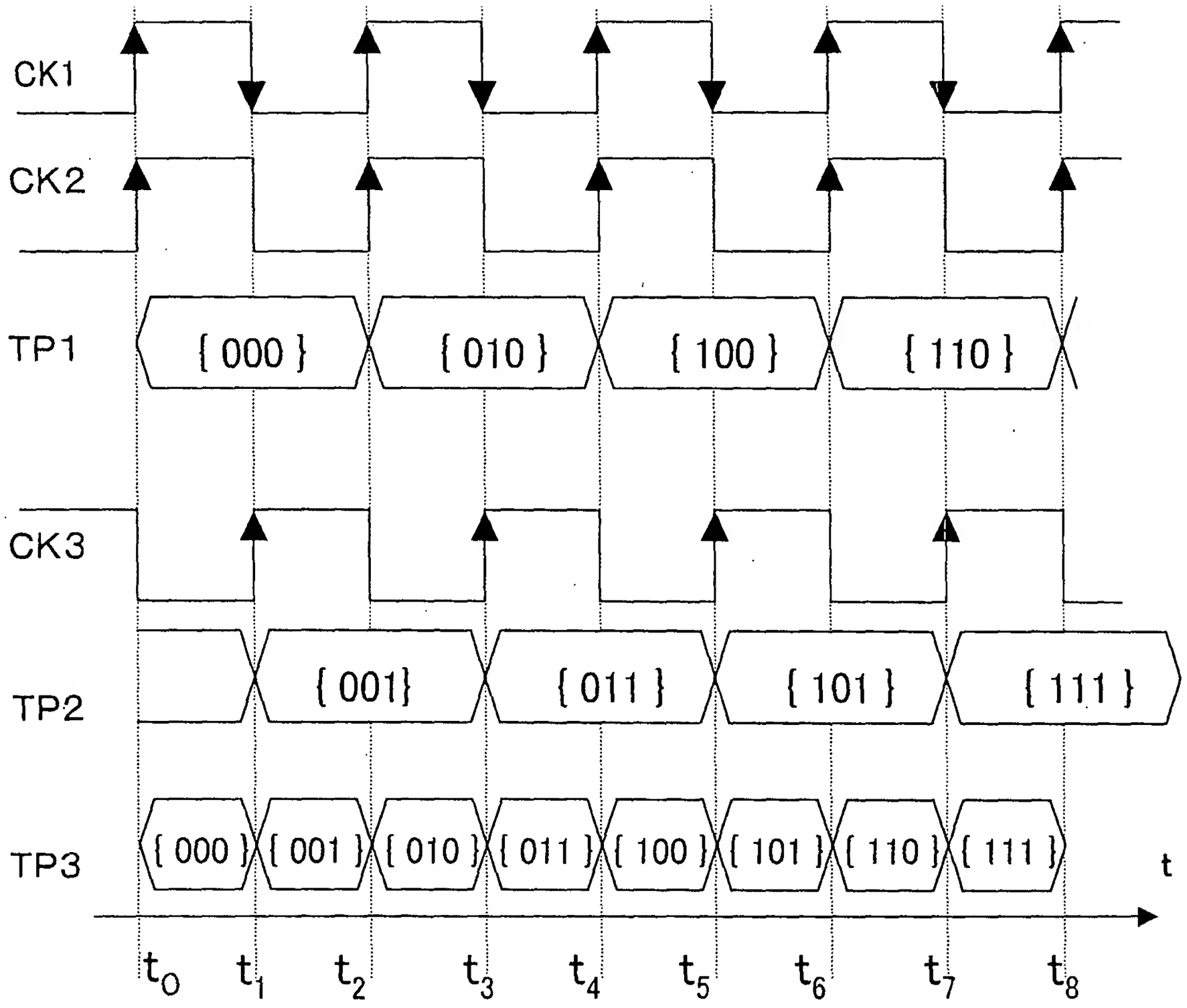

CK1
CK2
TP1
{ 000 }
{ 010 }
{ 100 }
{ 110 }
CK3
TP2
{ 001}
{ 011 }
{ 101 }
{ 111 }
TP3
{ 000 }
{ 001 }
{ 010 }
{ 011 }
{ 100 }
{ 101 }
{ 110 }
{ 111 }
t
t_0
t_1
t_2
t_3
t_4
t_5
t_6
t_7
t_8

FIG. 4

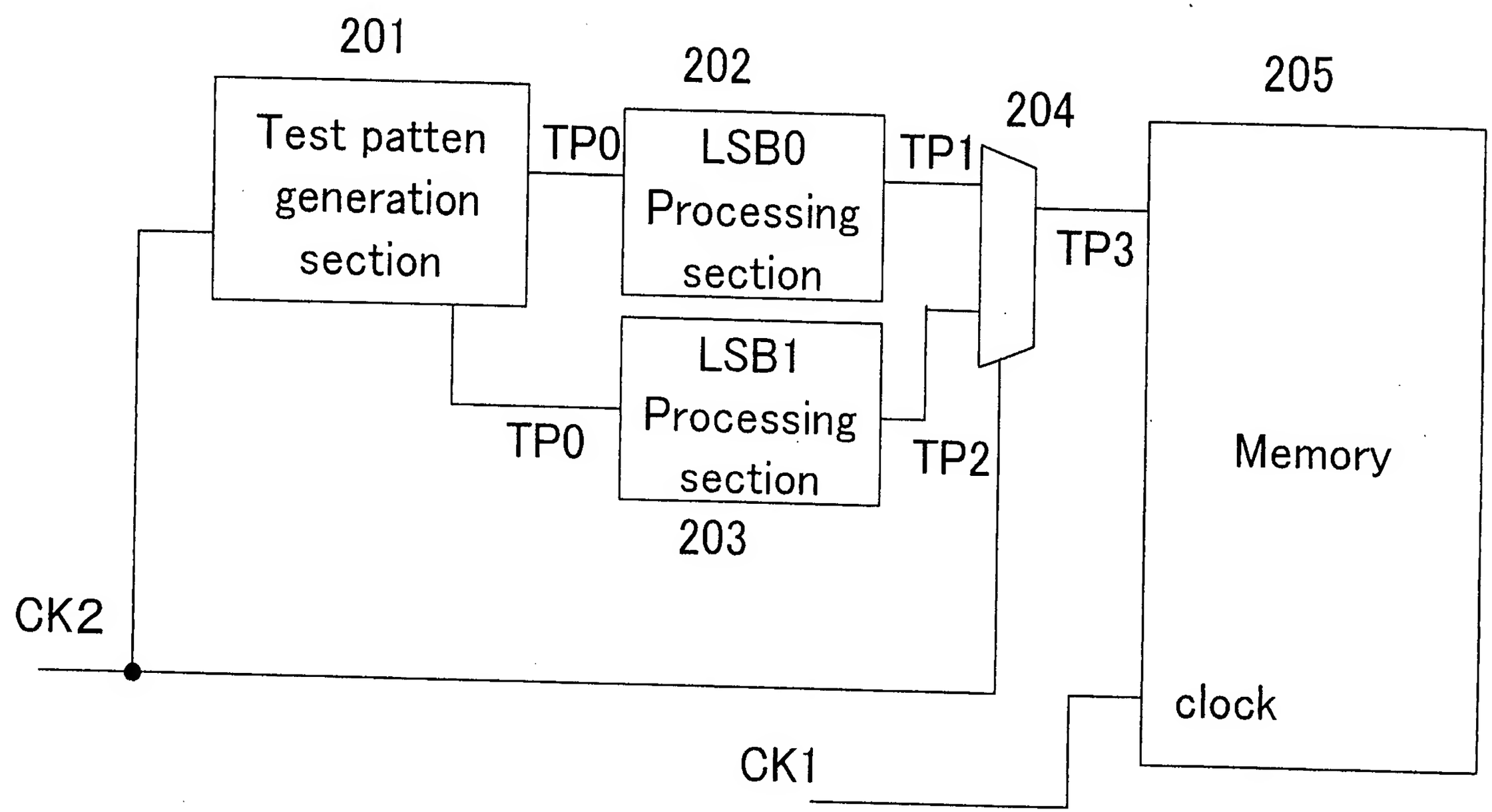

201
Test patten generation section
TP0
202
LSB0 Processing section
TP1
204
205
TP3
LSB1 Processing section
TP0
TP2
203
Memory
CK2
clock
CK1

FIG. 5

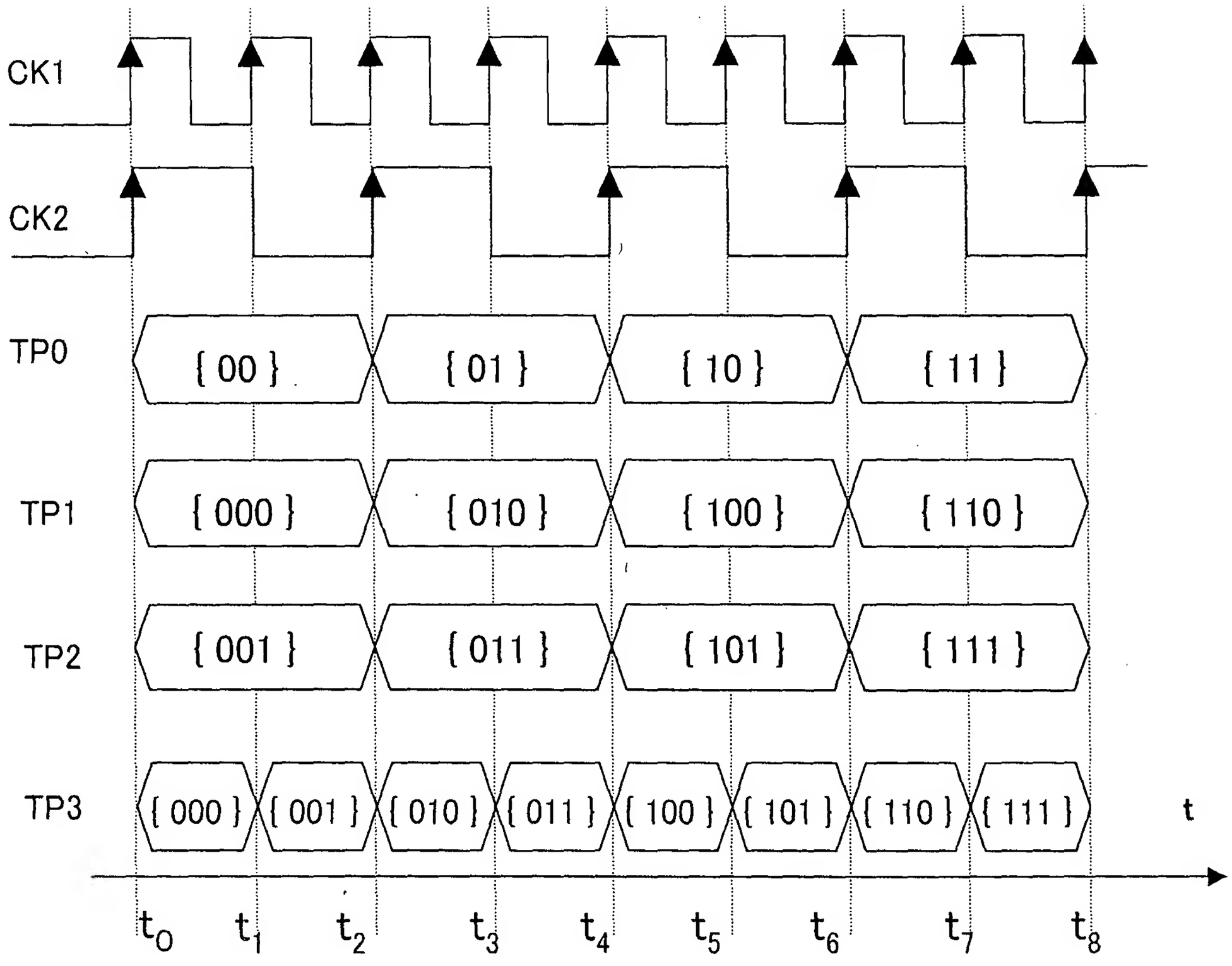

CK1
CK2
TP0
{ 00 }
{ 01 }
{ 10 }
{ 11 }
TP1
{ 000 }
{ 010 }
{ 100 }
{ 110 }
TP2
{ 001 }
{ 011 }
{ 101 }
{ 111 }
TP3
{ 000 }
{ 001 }
{ 010 }
{ 011 }
{ 100 }
{ 101 }
{ 110 }
{ 111 }
t
t_0
t_1
t_2
t_3
t_4
t_5
t_6
t_7
t_8

FIG. 6

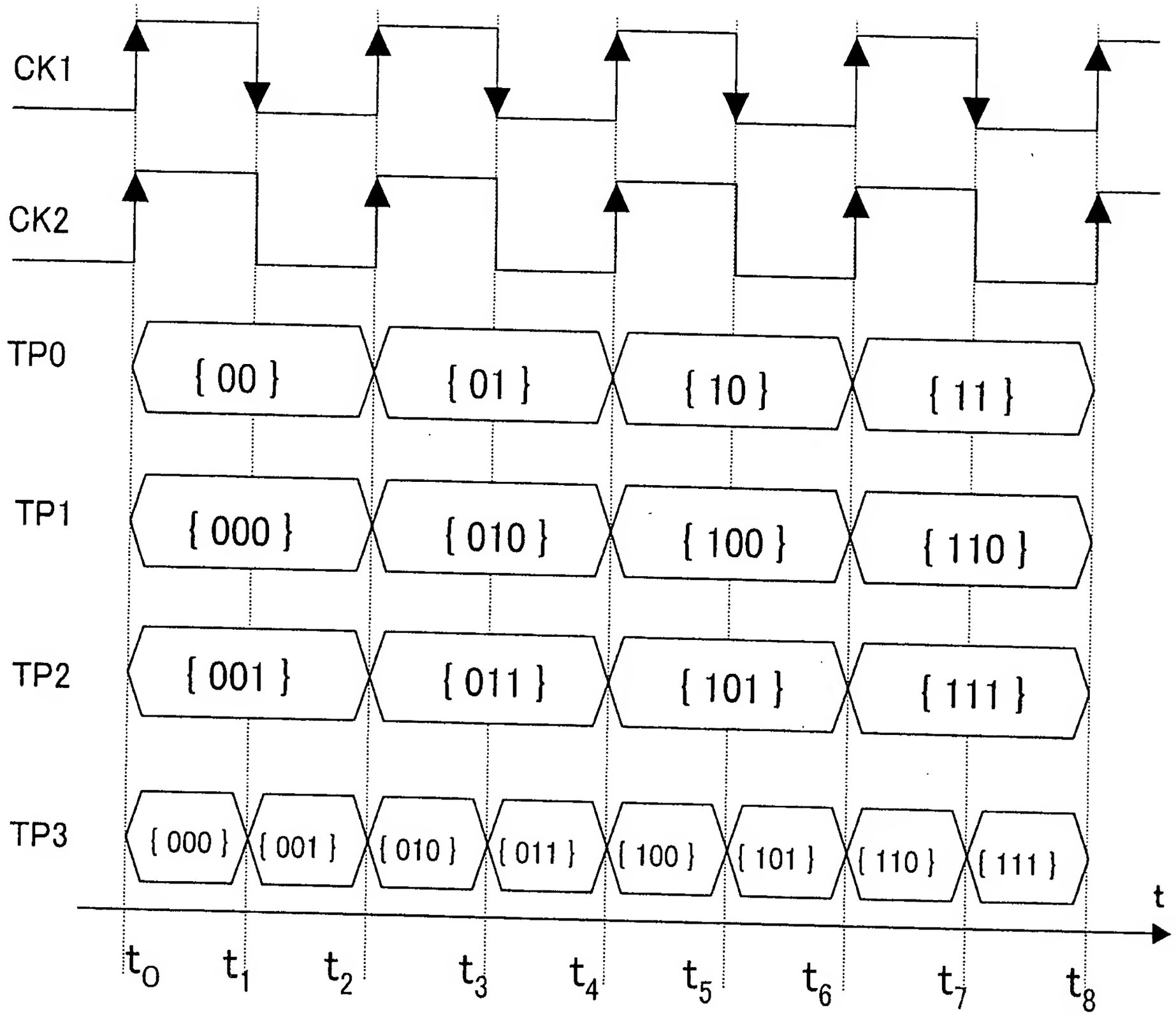

CK1
CK2
TP0
{ 00 }
{ 01 }
{ 10 }
{ 11 }
TP1
{ 000 }
{ 010 }
{ 100 }
{ 110 }
TP2
{ 001 }
{ 011 }
{ 101 }
{ 111 }
TP3
{ 000 }
{ 001 }
{ 010 }
{ 011 }
{ 100 }
{ 101 }
{ 110 }
{ 111 }
t
t_0
t_1
t_2
t_3
t_4
t_5
t_6
t_7
t_8

FIG. 7

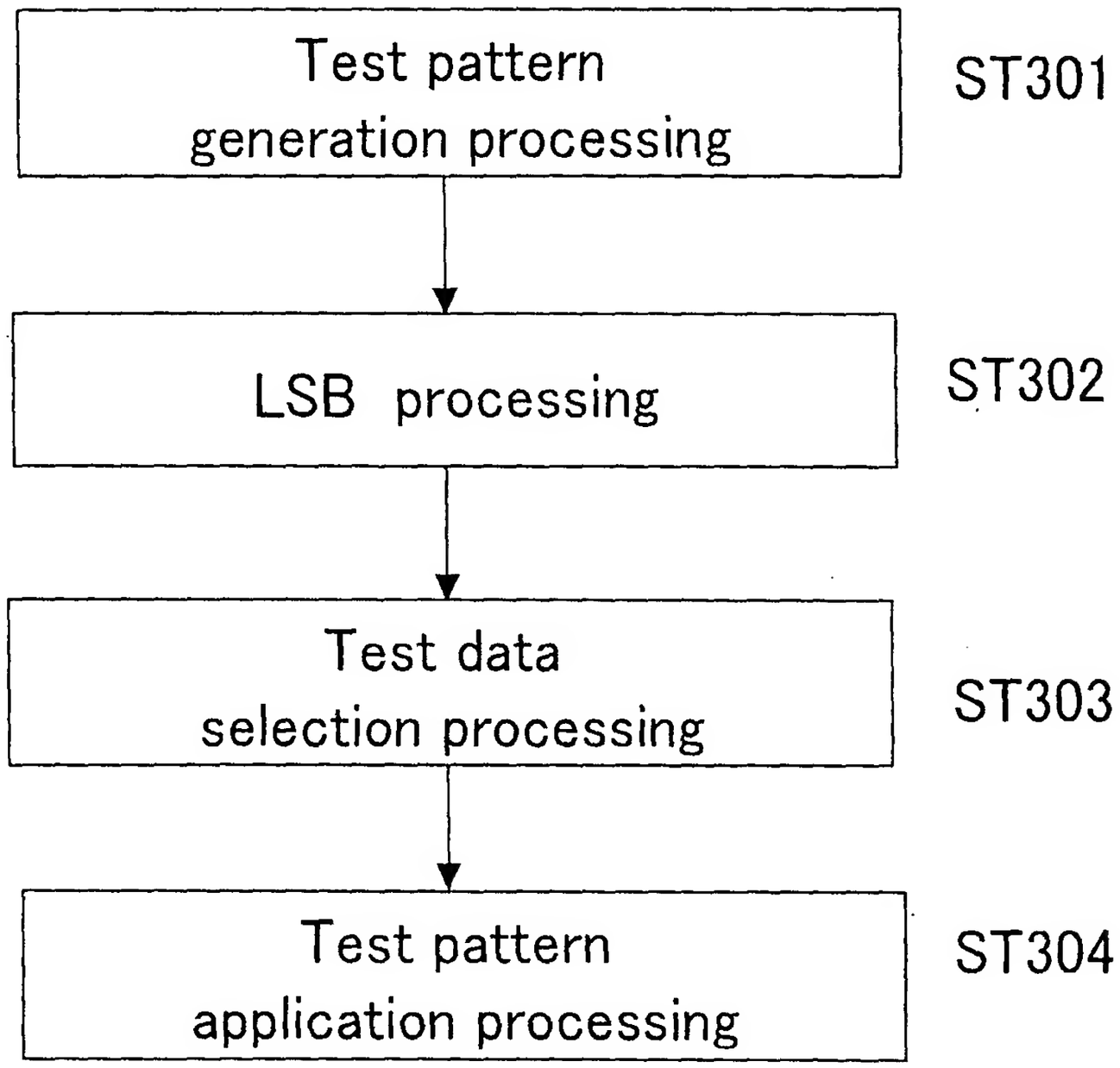

Test pattern generation processing
ST301
LSB processing
ST302
Test data selection processing
ST303
Test pattern application processing
ST304

FIG. 8

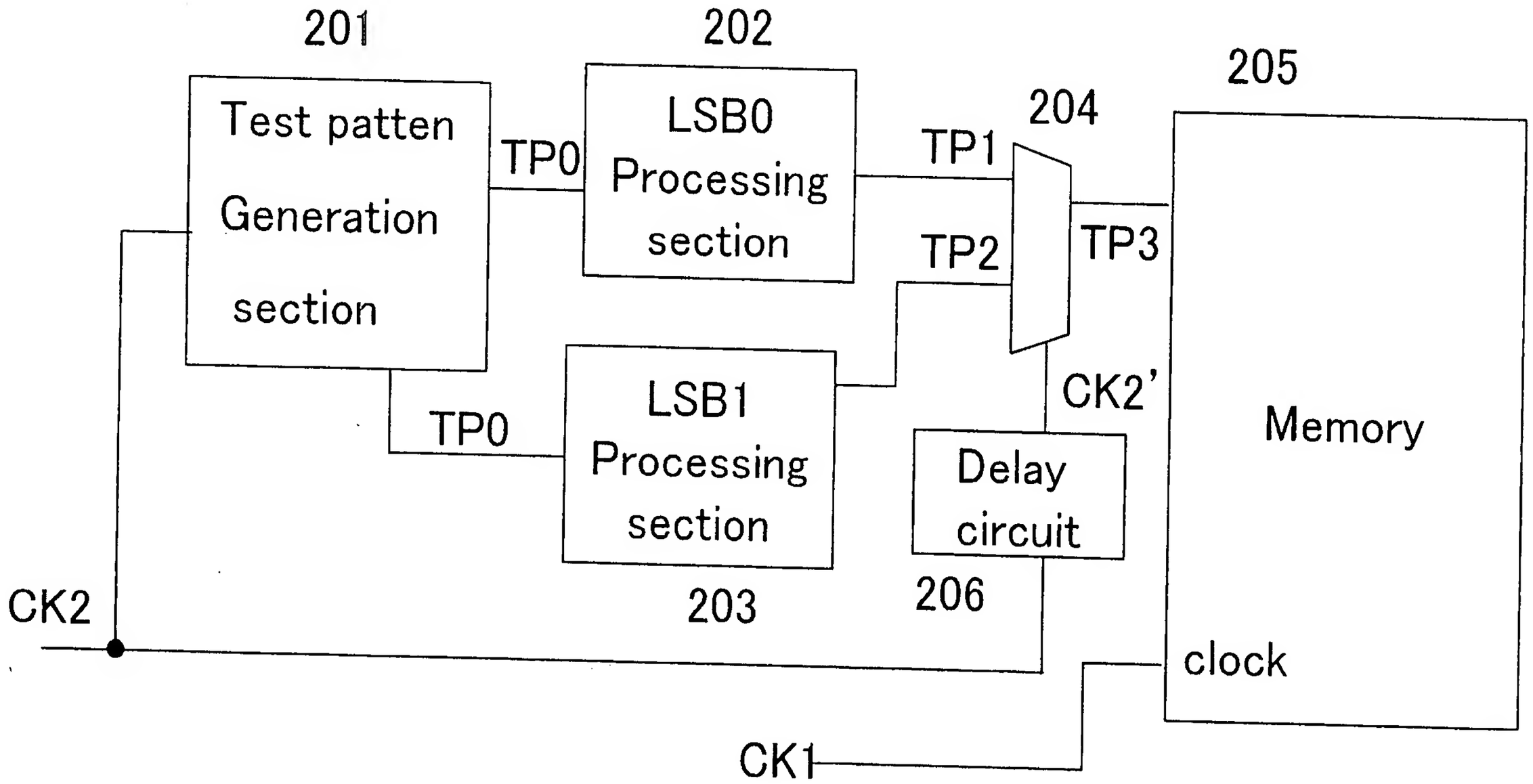

201
202
205
Test patten
Generation
section
TP0
LSB0
Processing
section
TP1
204
TP2
TP3
CK2'
Memory
TP0
LSB1
Processing
section
Delay
circuit
203
206
CK2
clock
CK1

FIG. 9

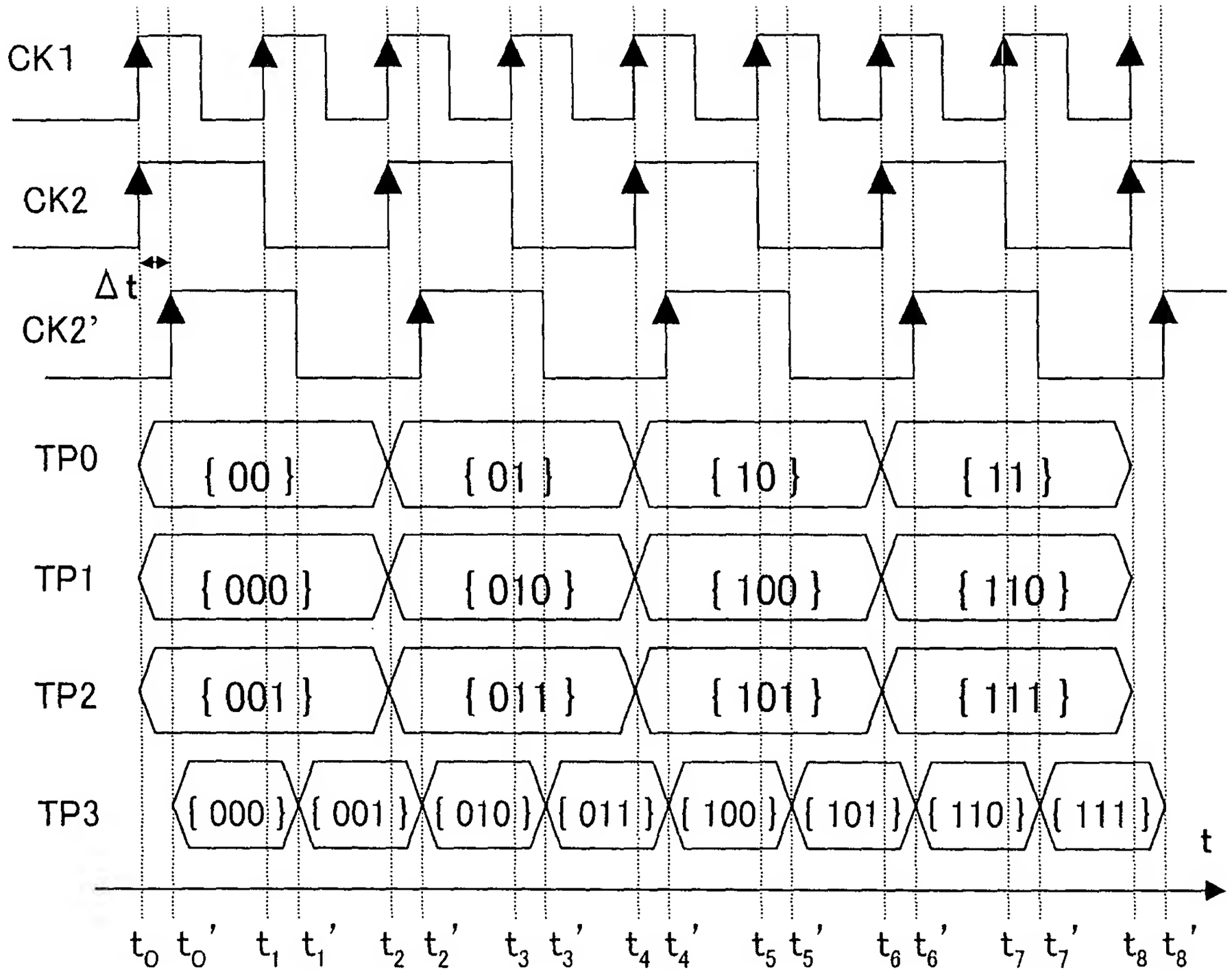

CK1
CK2
Δt
CK2'
TP0
{ 00 }
{ 01 }
{ 10 }
{ 11 }
TP1
{ 000 }
{ 010 }
{ 100 }
{ 110 }
TP2
{ 001 }
{ 011 }
{ 101 }
{ 111 }
TP3
{ 000 }
{ 001 }
{ 010 }
{ 011 }
{ 100 }
{ 101 }
{ 110 }
{ 111 }
t
t0 t0' t1 t1' t2 t2' t3 t3' t4 t4' t5 t5' t6 t6' t7 t7' t8 t8'

FIG. 10

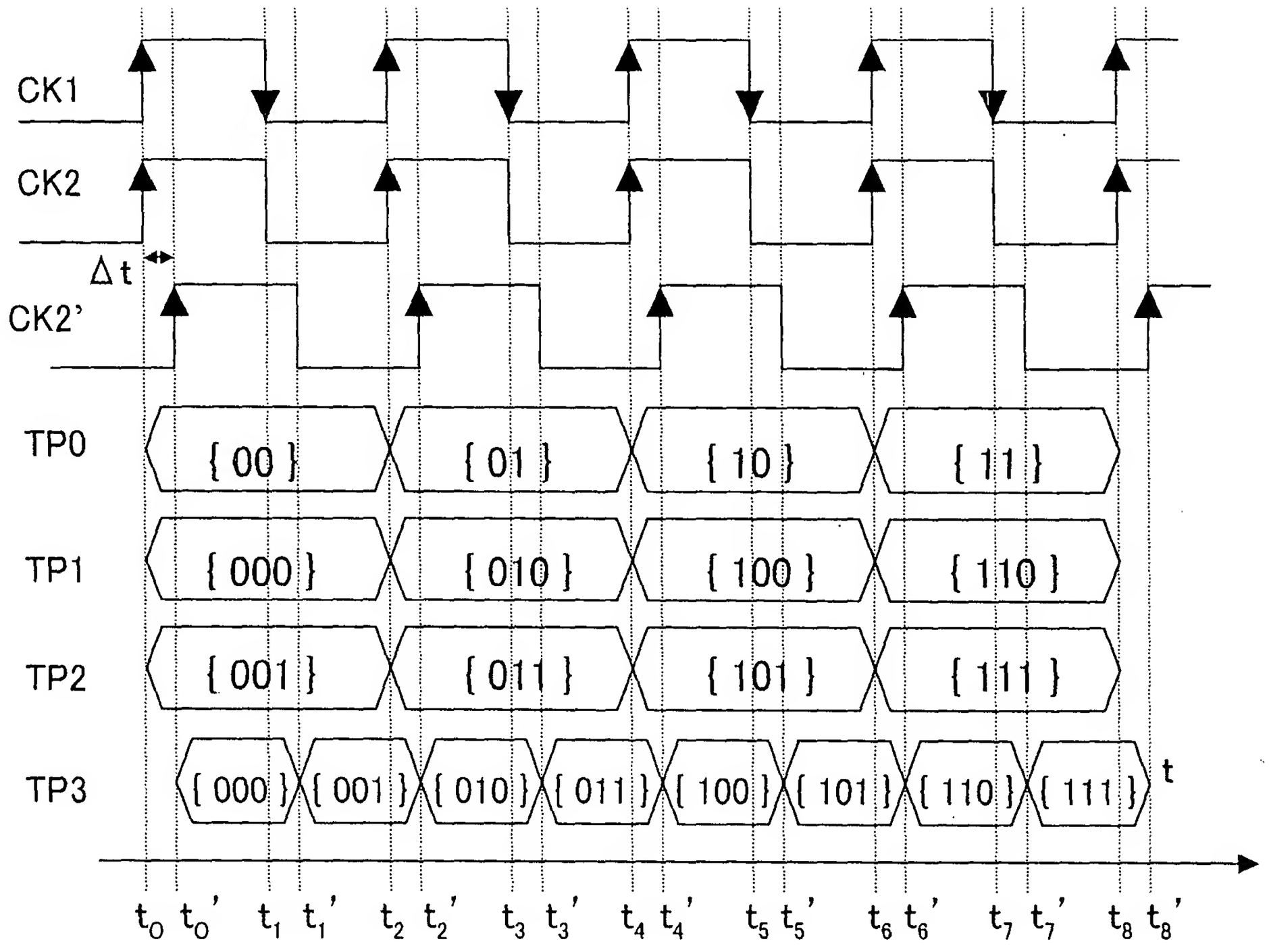

CK1
CK2
Δt
CK2'
TP0
{ 00 }
{ 01 }
{ 10 }
{ 11 }
TP1
{ 000 }
{ 010 }
{ 100 }
{ 110 }
TP2
{ 001 }
{ 011 }
{ 101 }
{ 111 }
TP3
{ 000 }
{ 001 }
{ 010 }
{ 011 }
{ 100 }
{ 101 }
{ 110 }
{ 111 }
t
t0 t0' t1 t1' t2 t2' t3 t3' t4 t4' t5 t5' t6 t6' t7 t7' t8 t8'

FIG. 11

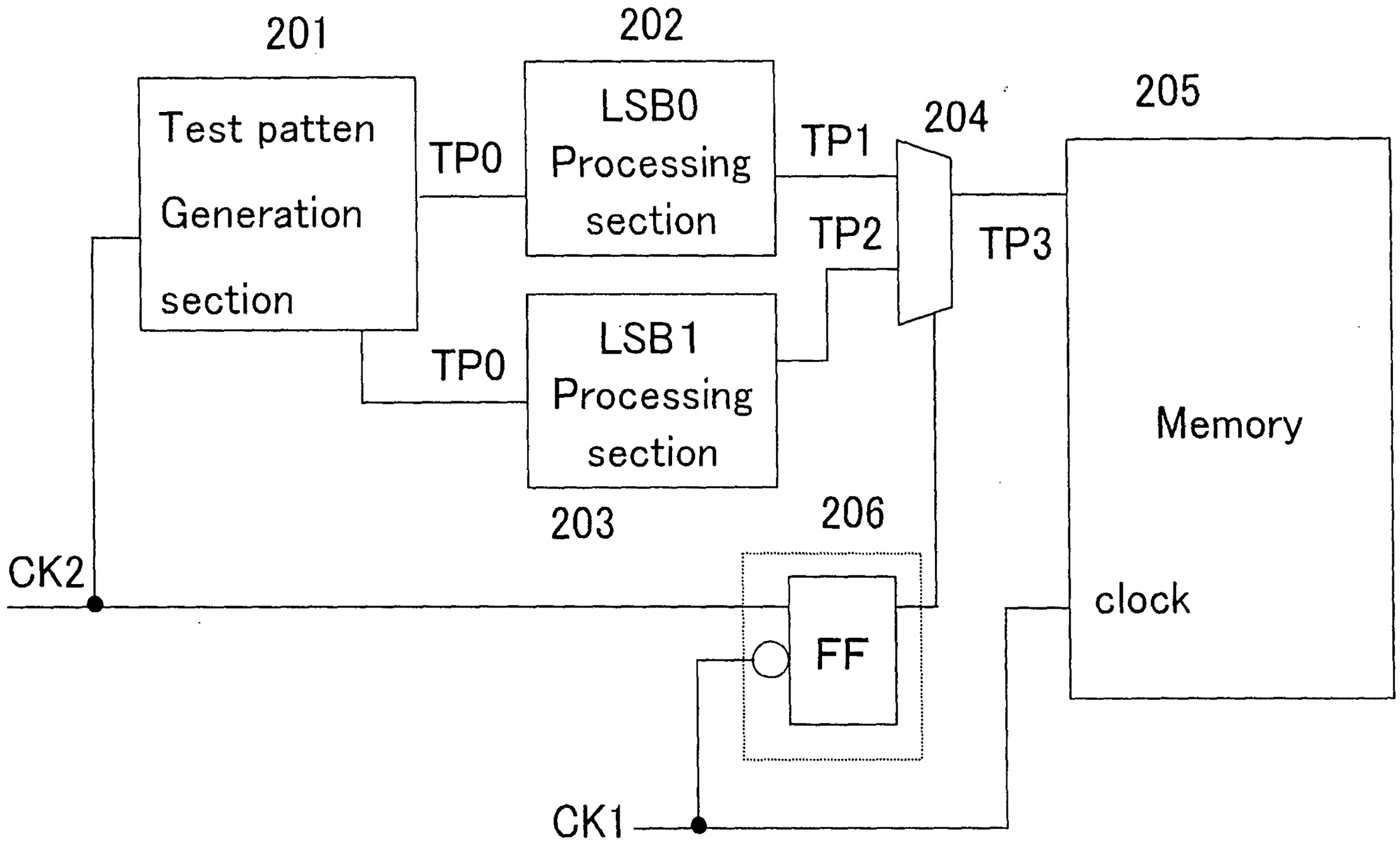

201
202
205
Test patten
Generation
section
TP0
LSB0
Processing
section
TP1
204
TP2
TP3
TP0
LSB1
Processing
section
Memory
203
206
CK2
clock
FF
CK1

FIG. 12

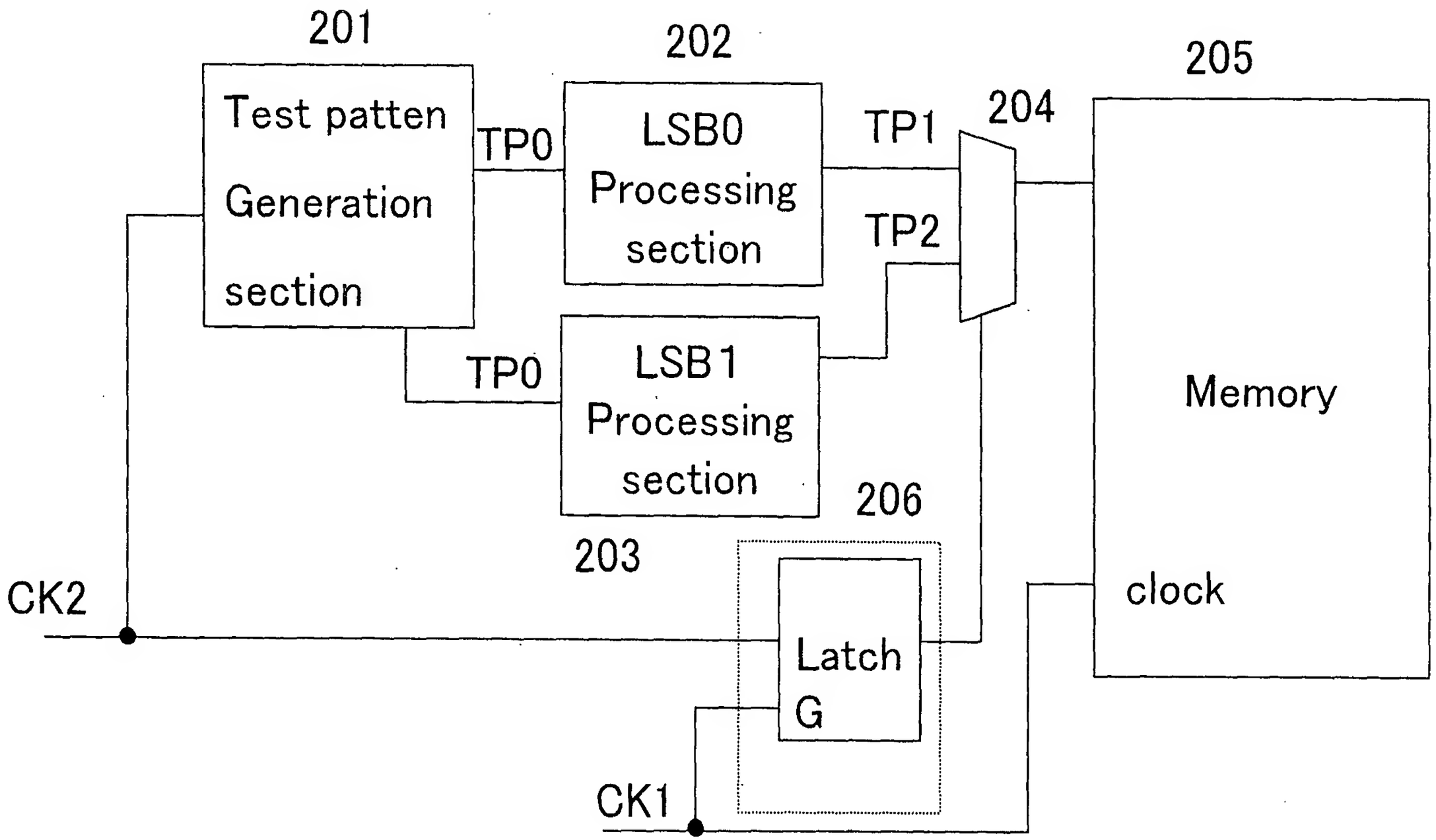

201
Test patten Generation section
TP0
202
LSB0 Processing section
TP1
204
205
Memory
clock
TP2
TP0
LSB1 Processing section
206
203
CK2
Latch G
CK1

FIG. 13

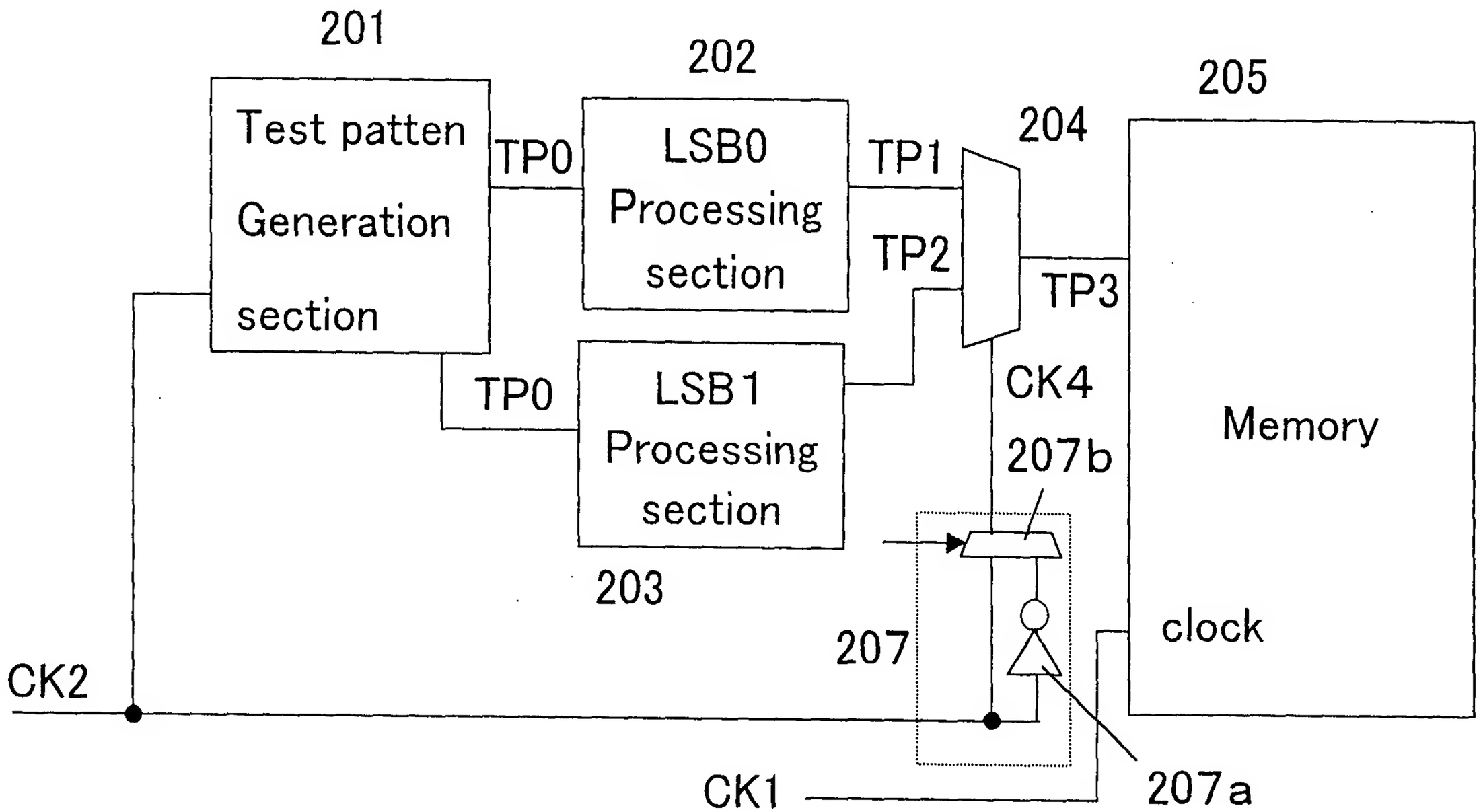

201
Test patten
Generation
section
202
LSB0
Processing
section
TP0
TP1
204
205
TP2
TP3
CK4
Memory
207b
TP0
LSB1
Processing
section
203
207
clock
CK2
CK1
207a

FIG. 14

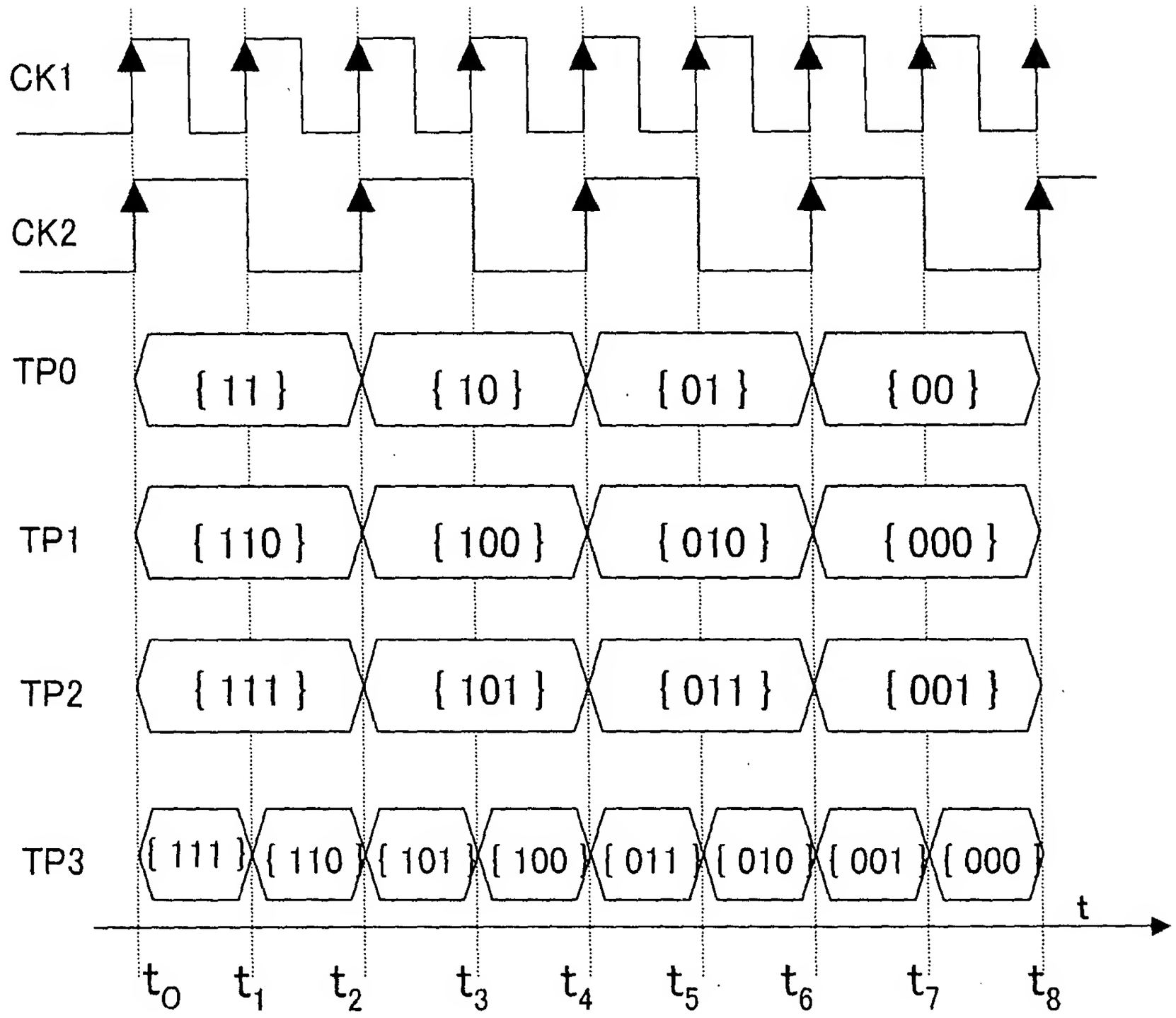

CK1
CK2
TP0
{ 11 }
{ 10 }
{ 01 }
{ 00 }
TP1
{ 110 }
{ 100 }
{ 010 }
{ 000 }
TP2
{ 111 }
{ 101 }
{ 011 }
{ 001 }
TP3
{ 111 }
{ 110 }
{ 101 }
{ 100 }
{ 011 }
{ 010 }
{ 001 }
{ 000 }
t
t_0 t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8

FIG. 15

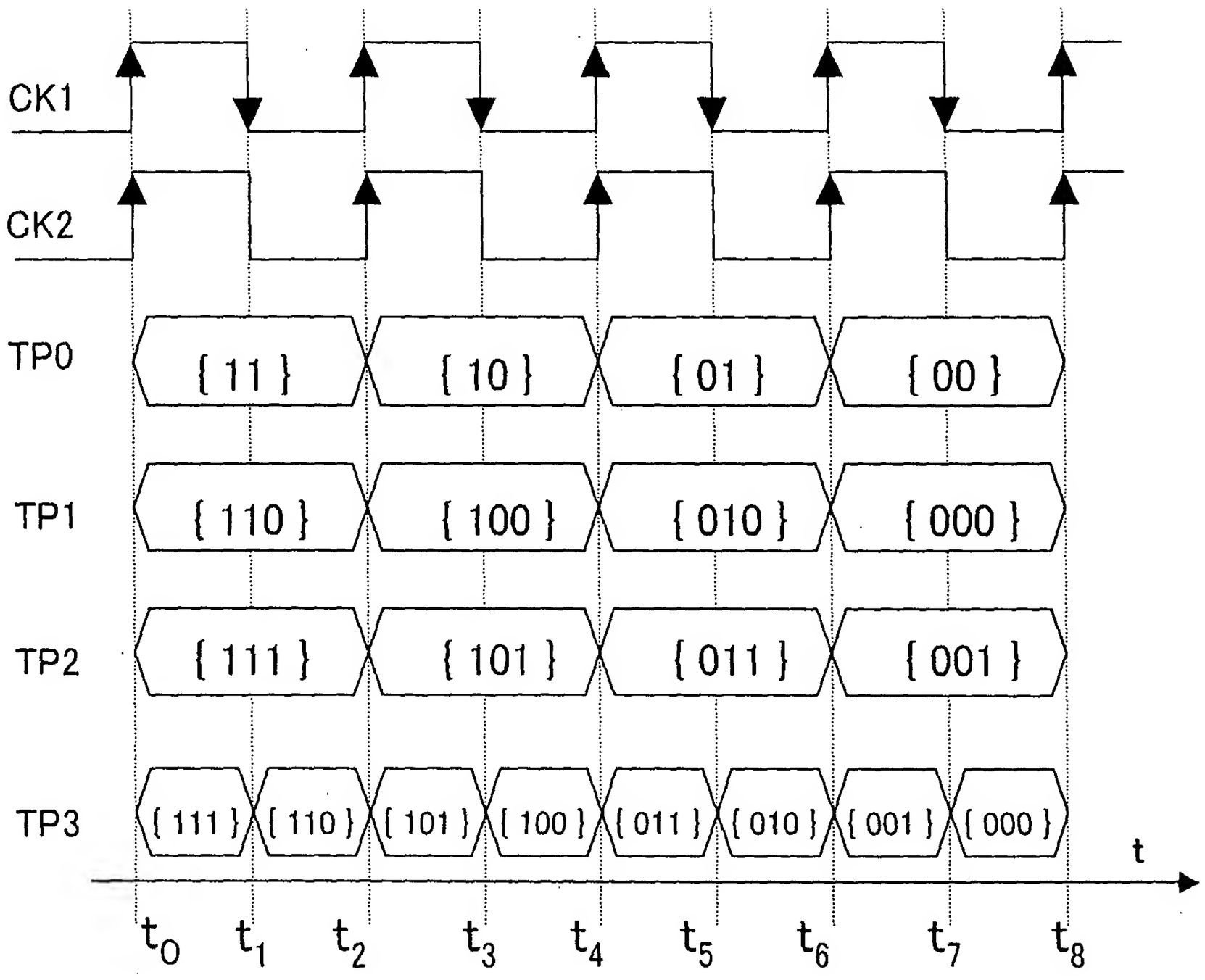

CK1
CK2
TP0
{ 11 }
{ 10 }
{ 01 }
{ 00 }
TP1
{ 110 }
{ 100 }
{ 010 }
{ 000 }
TP2
{ 111 }
{ 101 }
{ 011 }
{ 001 }
TP3
{ 111 }
{ 110 }
{ 101 }
{ 100 }
{ 011 }
{ 010 }
{ 001 }
{ 000 }
t
t_0 t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8

FIG. 16

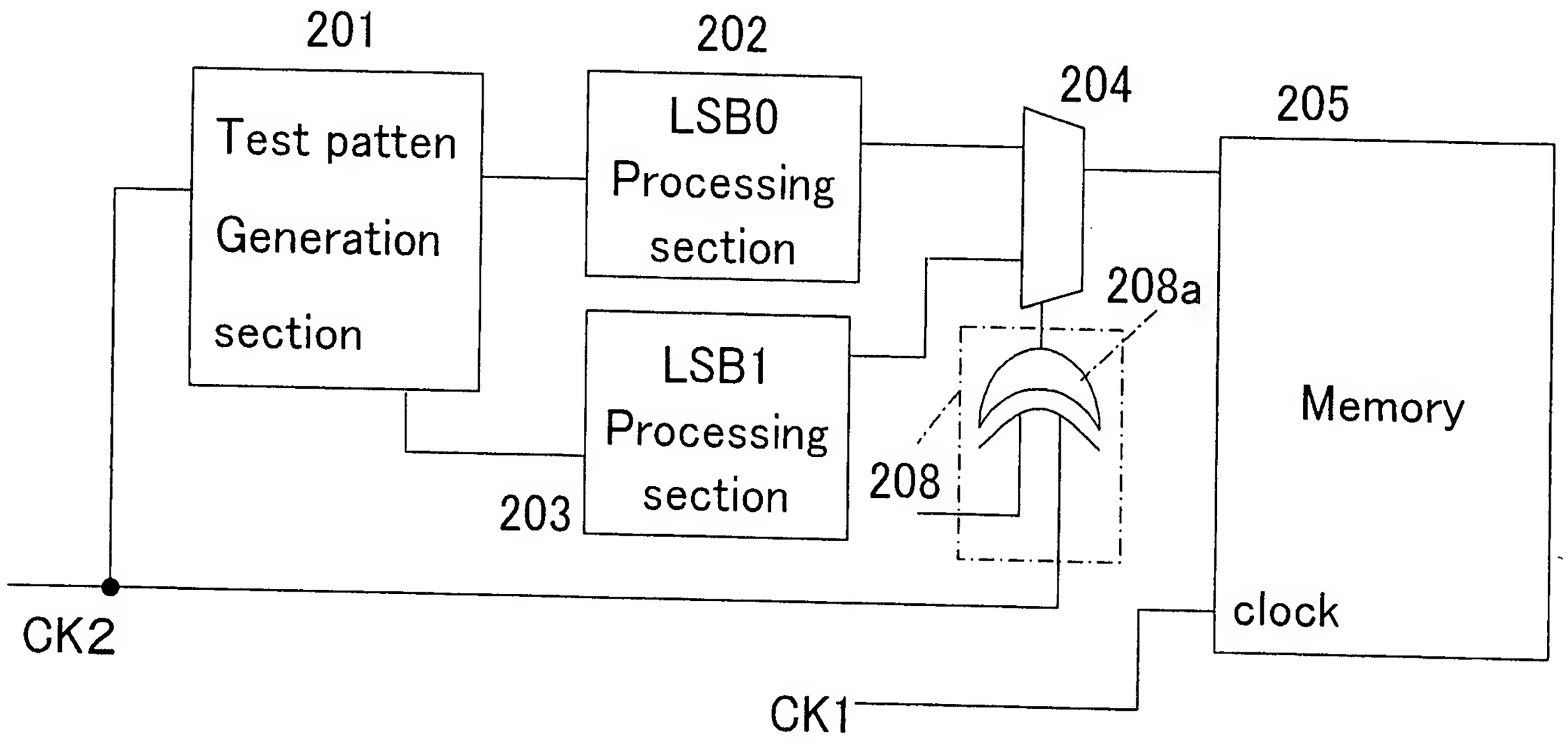

201
202
204
205
Test patten
Generation
section
LSB0
Processing
section
LSB1
Processing
section
203
208a
208
Memory
clock
CK2
CK1

FIG. 17

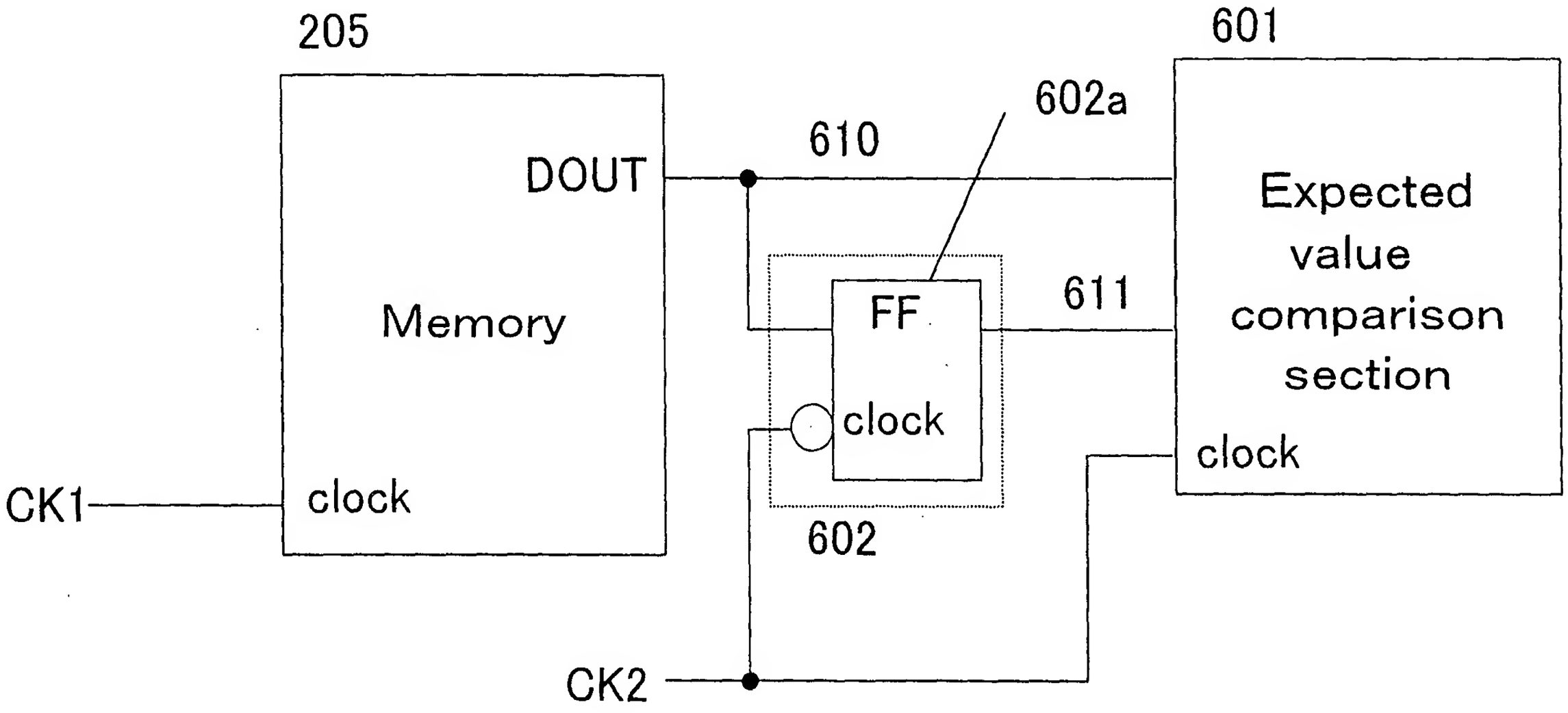

205
601
602a
610
DOUT
Memory
clock
CK1
FF
clock
611
602
Expected value comparison section
clock
CK2

FIG. 18

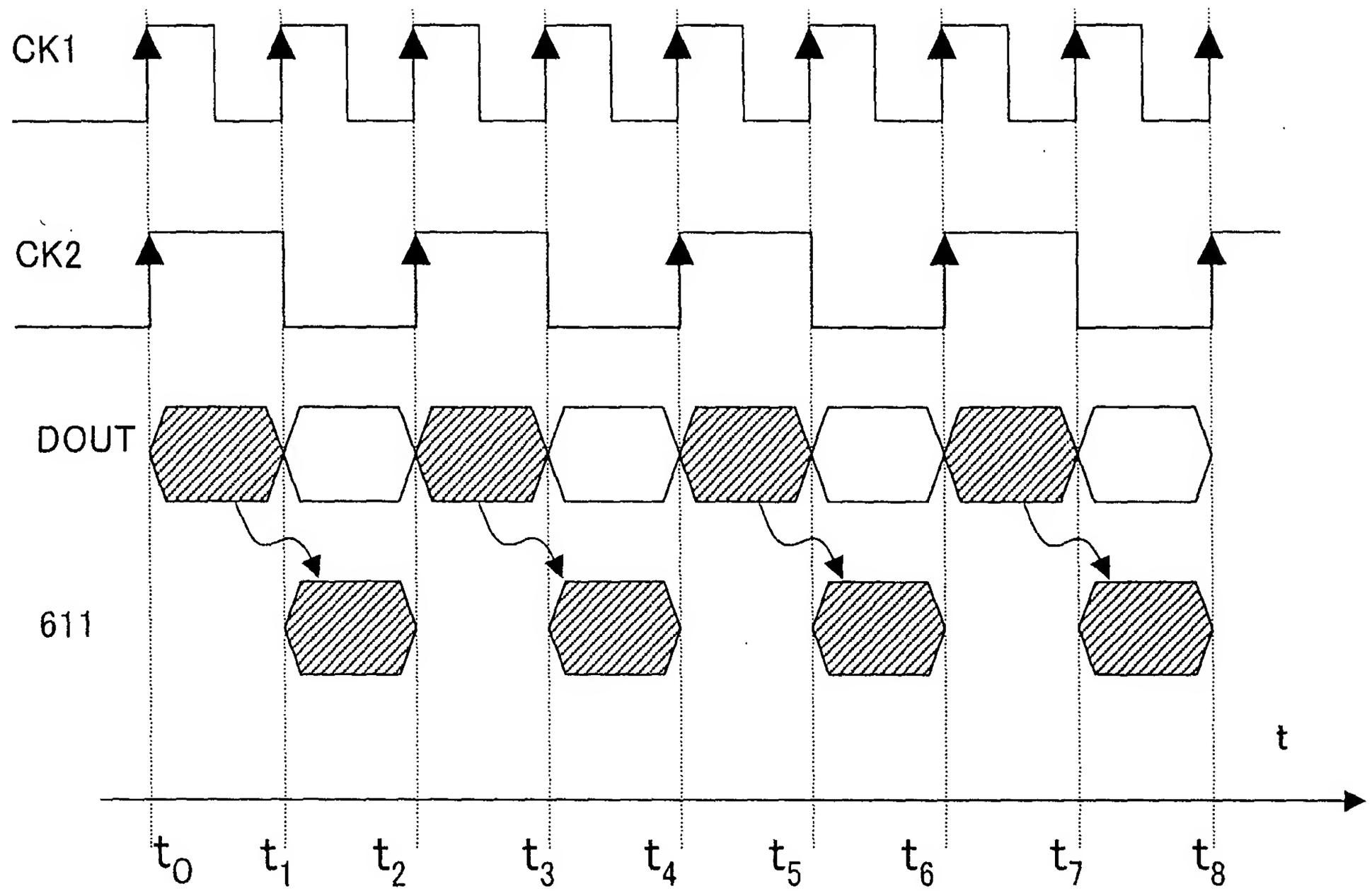


FIG. 19

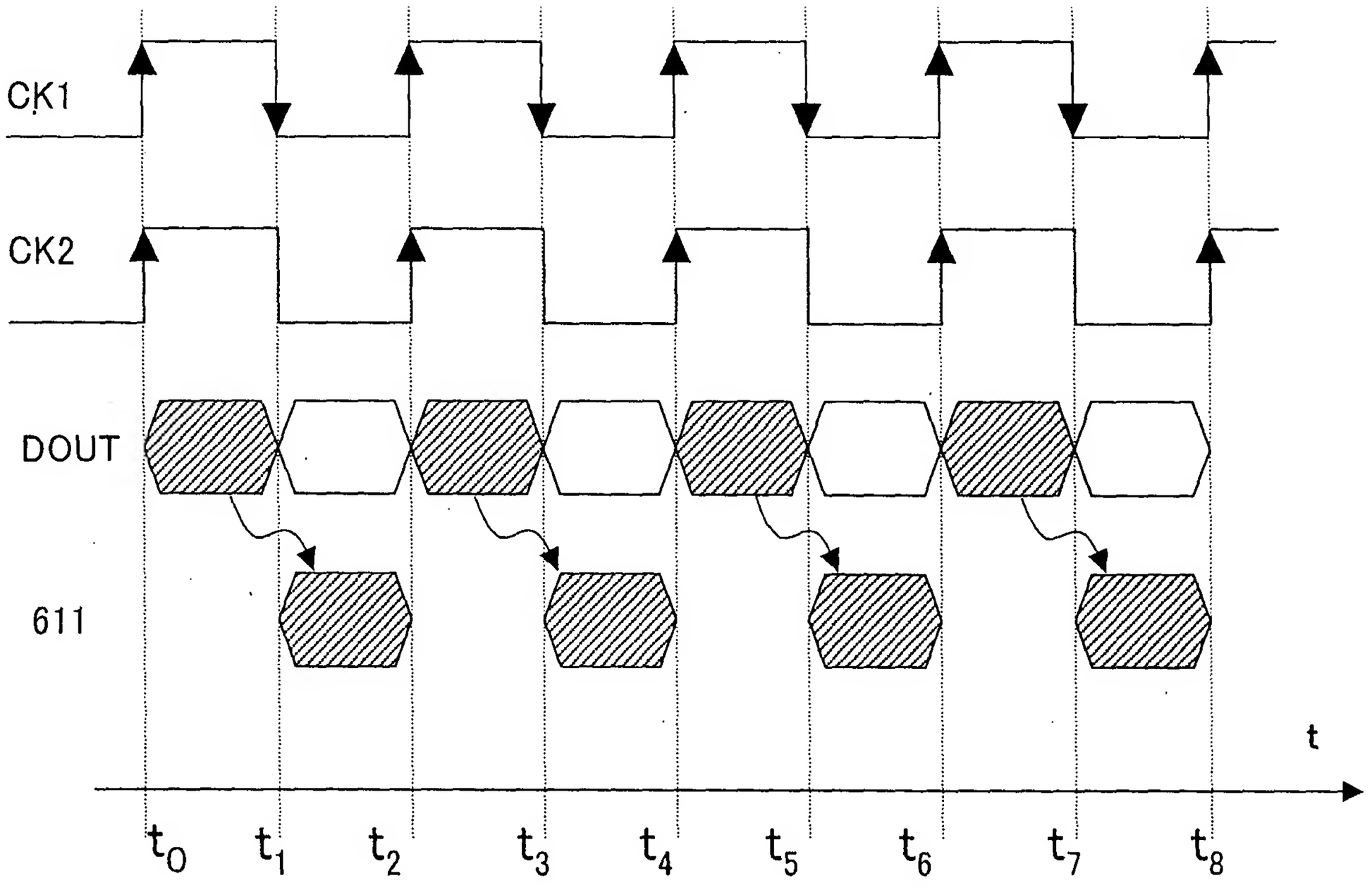


FIG. 20

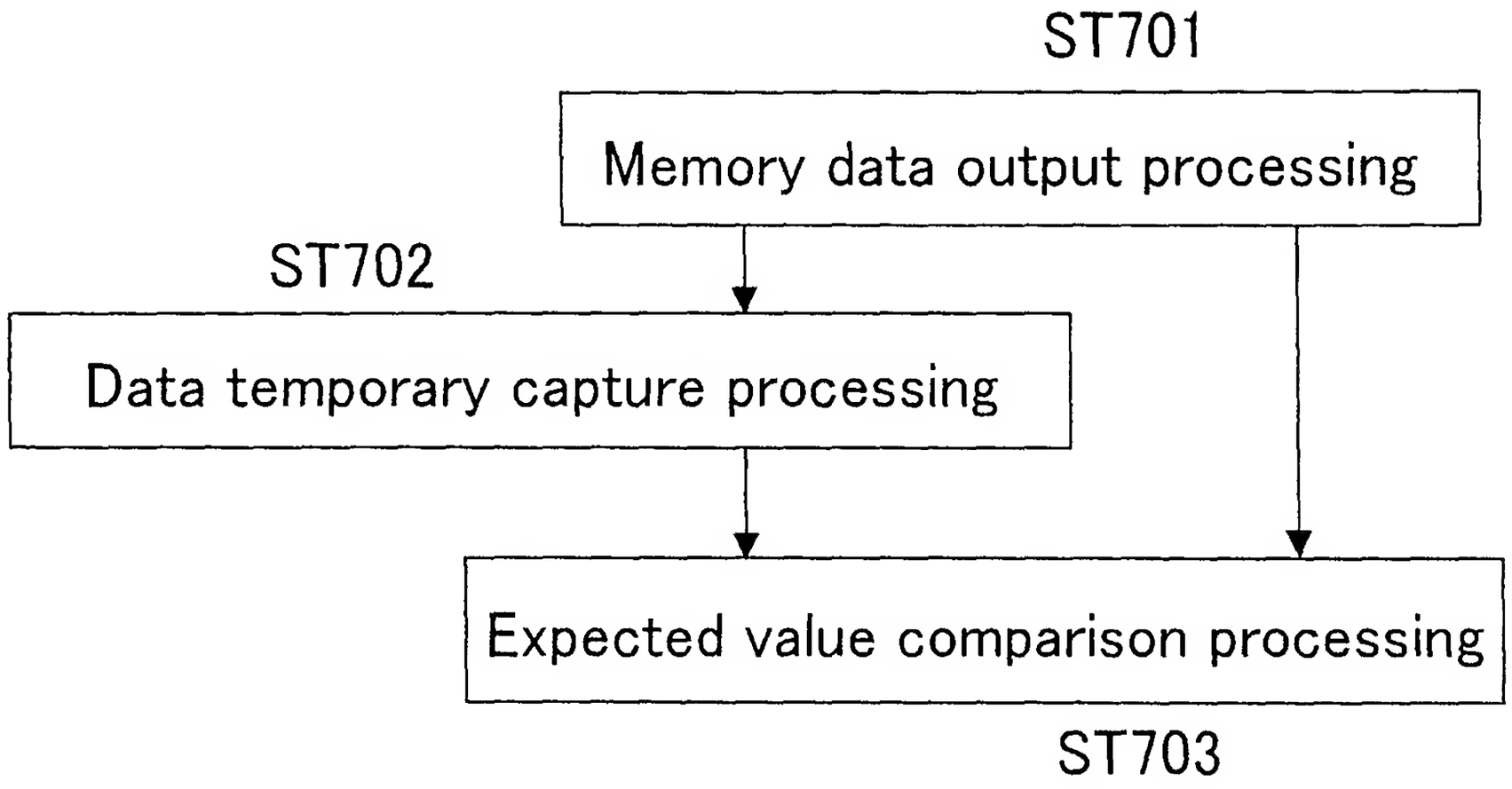

ST701
Memory data output processing
ST702
Data temporary capture processing
Expected value comparison processing
ST703

FIG. 21

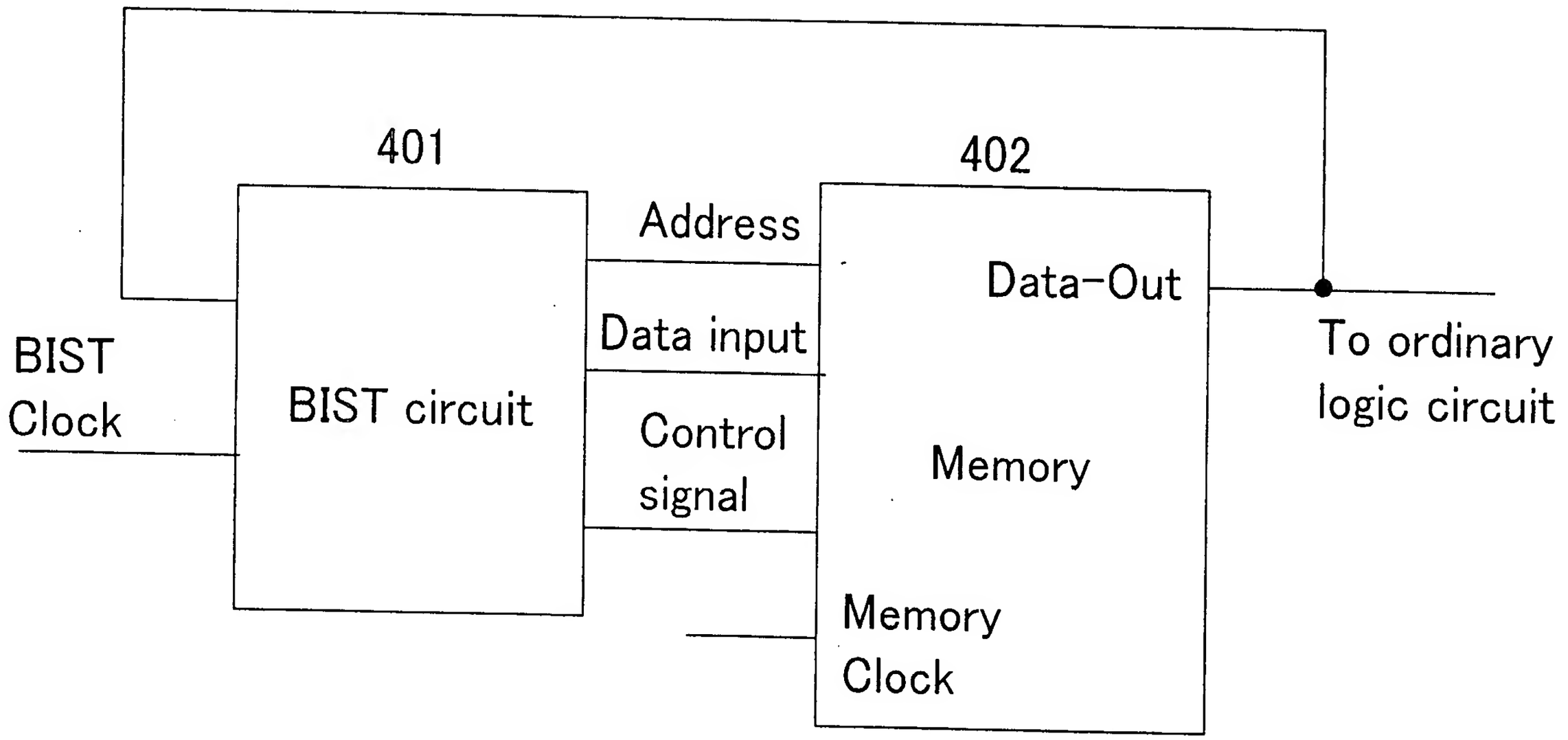

401
402
Address
Data-Out
Data input
BIST
Clock
BIST circuit
Control
signal
Memory
Memory
Clock
To ordinary
logic circuit

FIG. 22

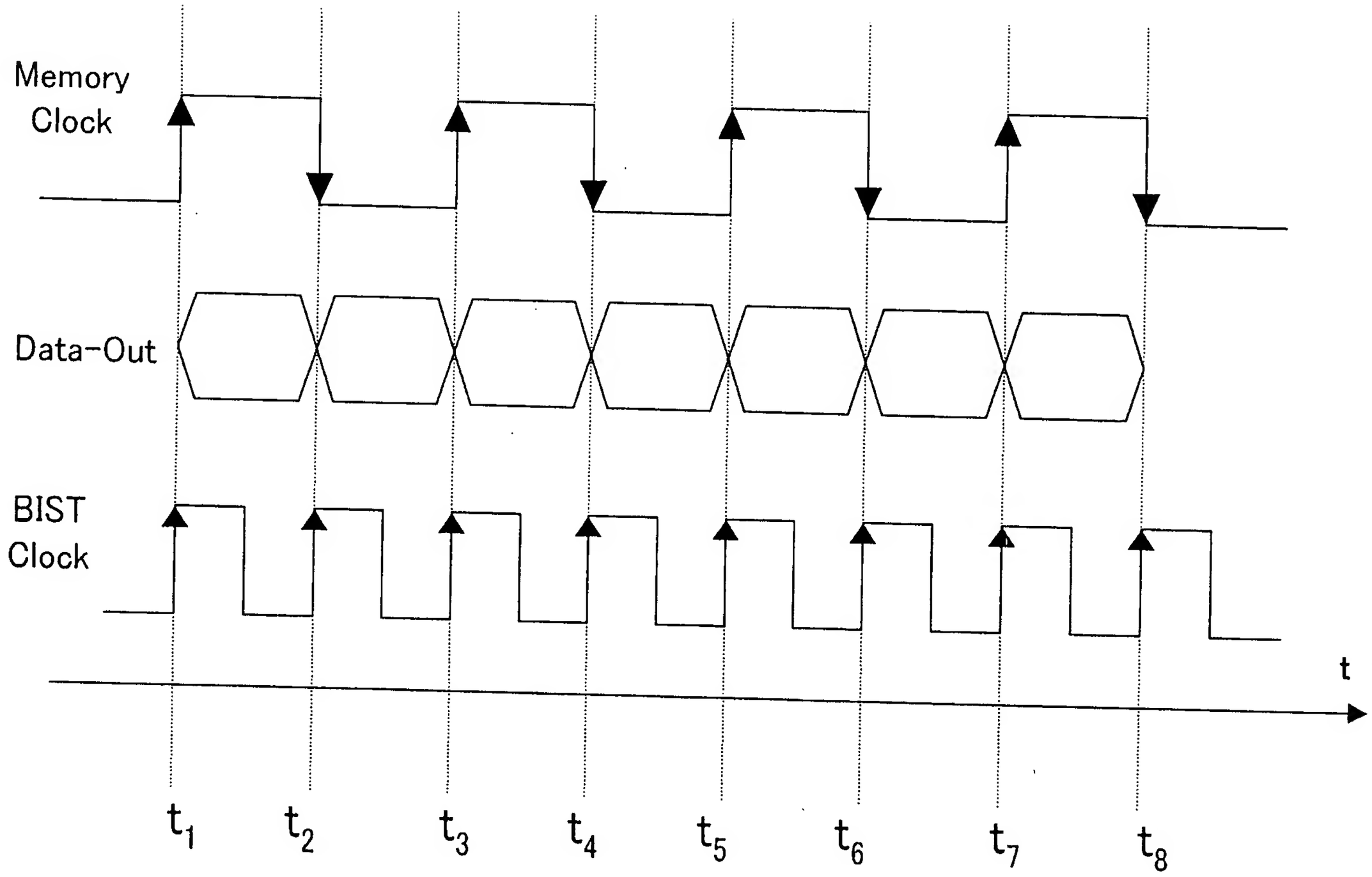


FIG. 23

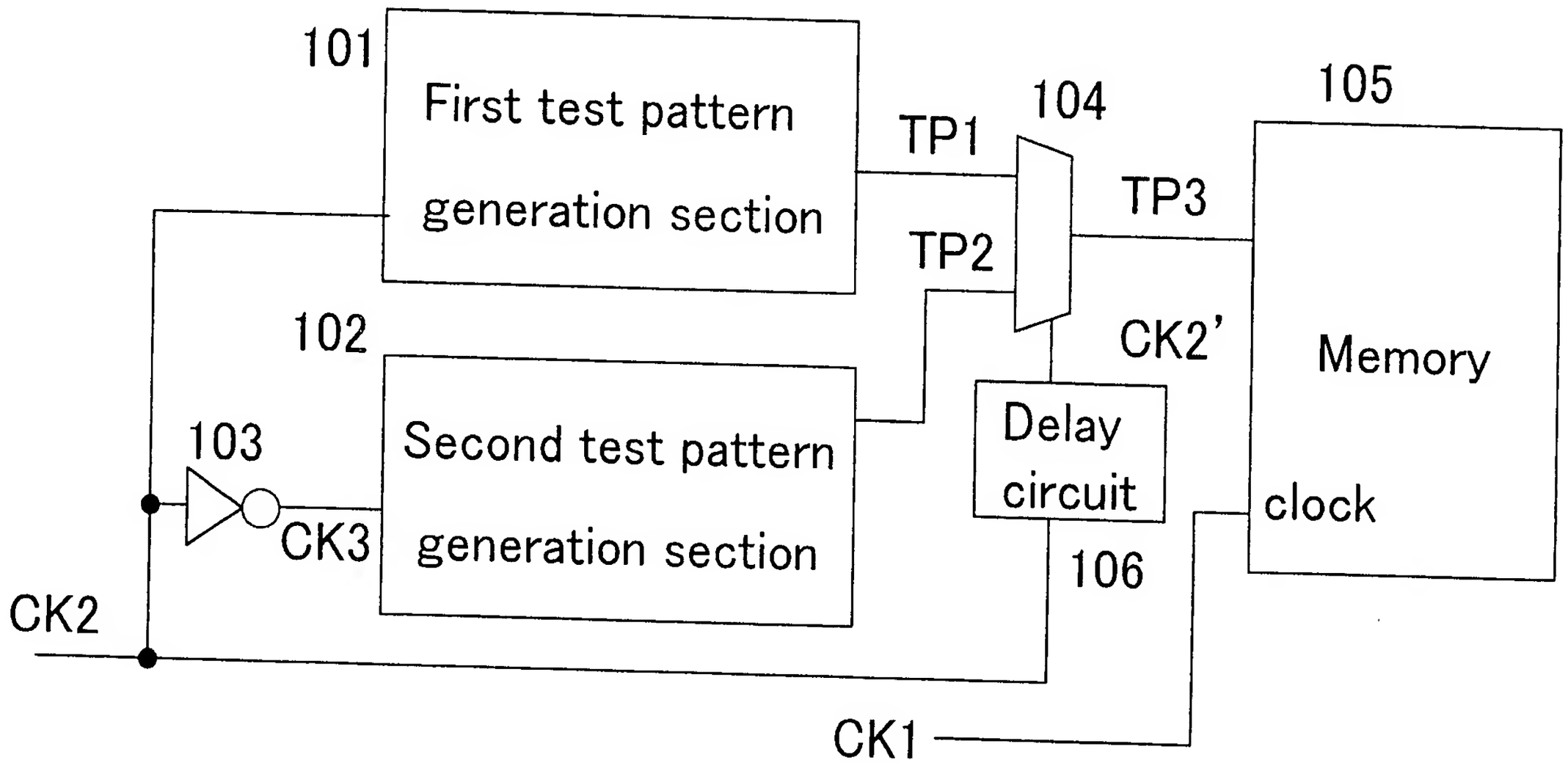

101
First test pattern generation section
TP1
104
105
TP3
TP2
CK2'
Memory
102
Delay circuit
103
Second test pattern generation section
clock
CK3
106
CK2
CK1

FIG. 24

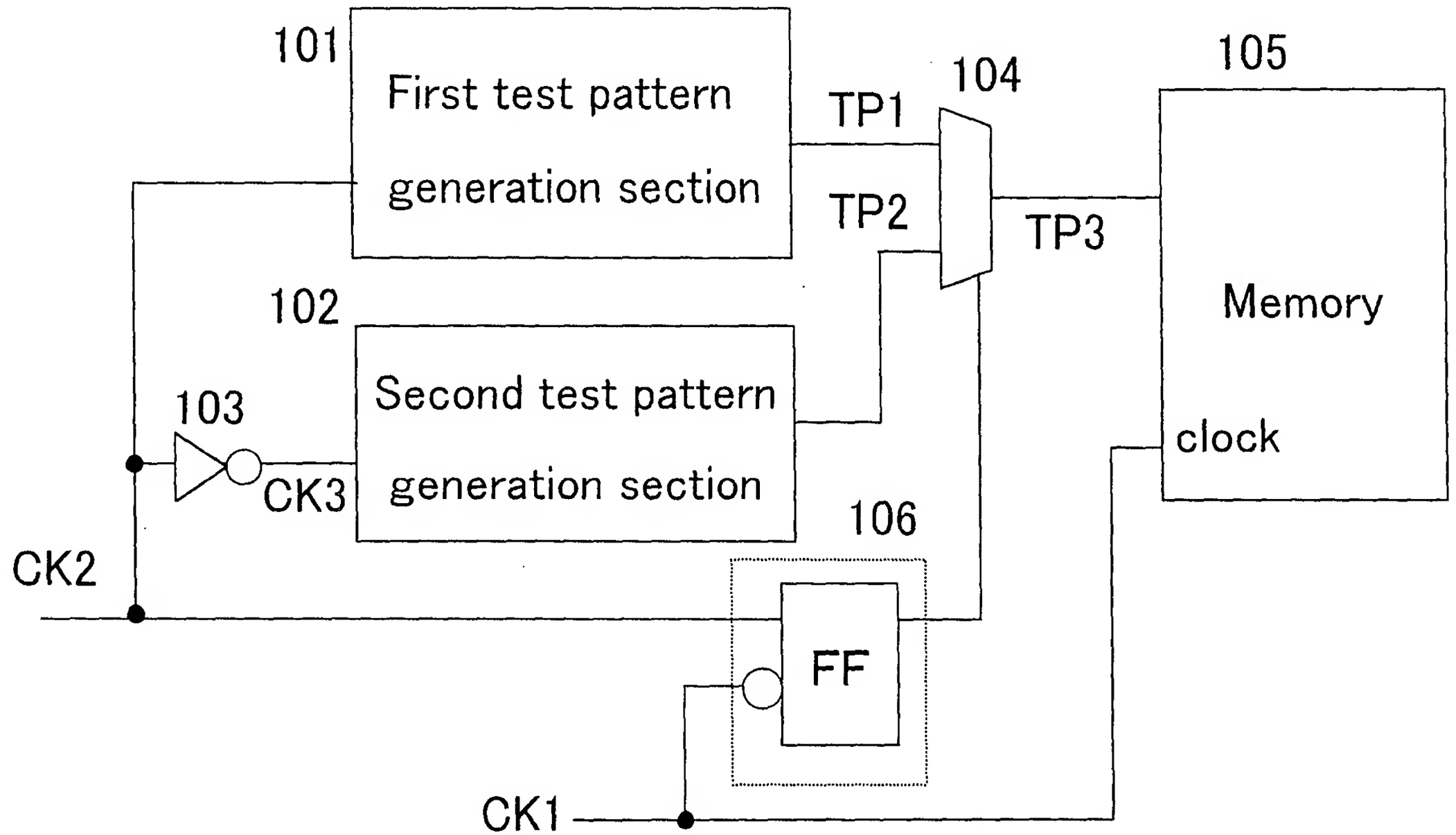

101
First test pattern generation section
TP1
104
105
TP2
TP3
Memory
102
Second test pattern generation section
103
CK3
clock
106
CK2
FF
CK1

FIG. 25

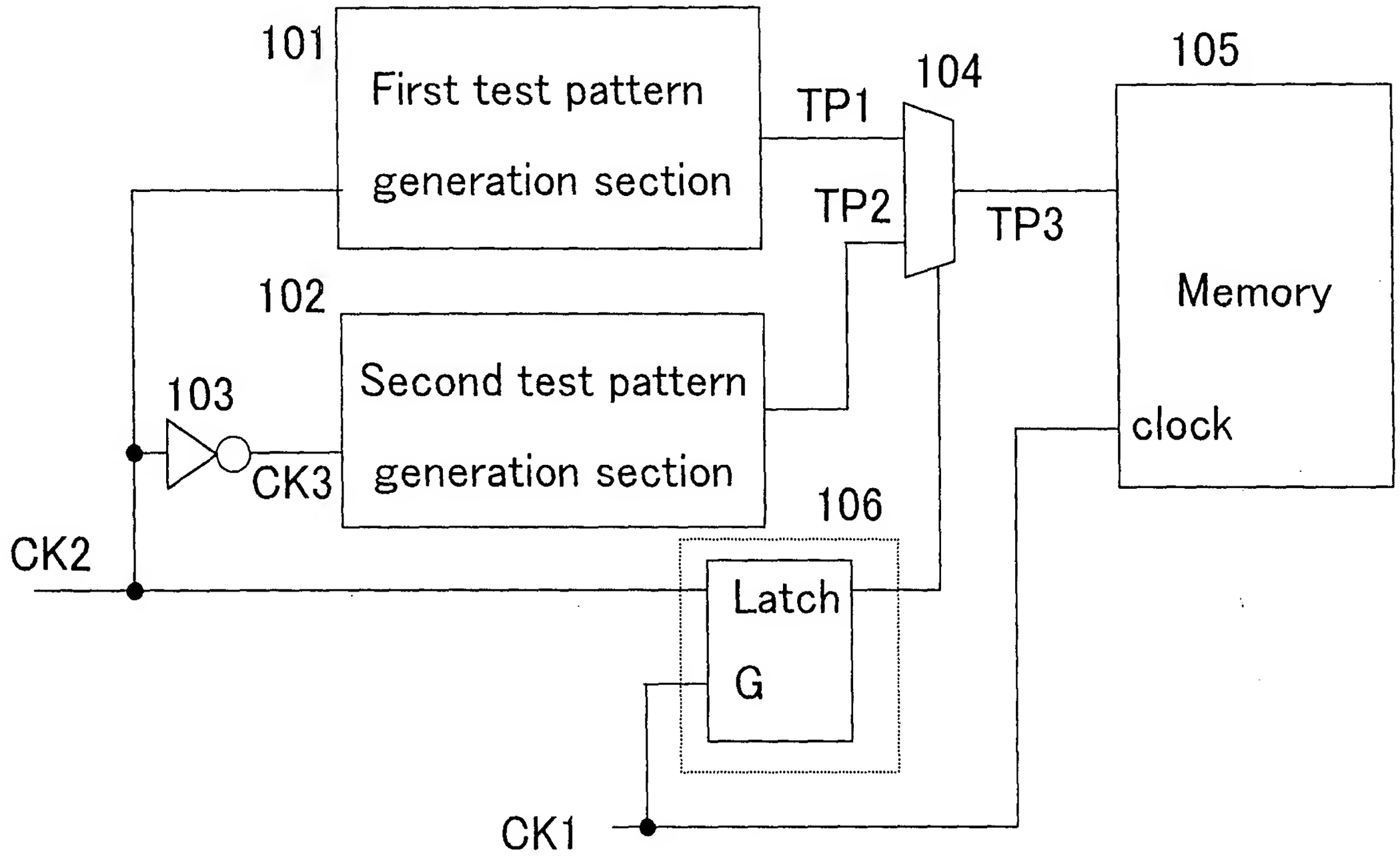

101
First test pattern generation section
TP1
104
105
TP2
TP3
Memory
102
Second test pattern generation section
clock
103
CK3
106
CK2
Latch
G
CK1

FIG. 26

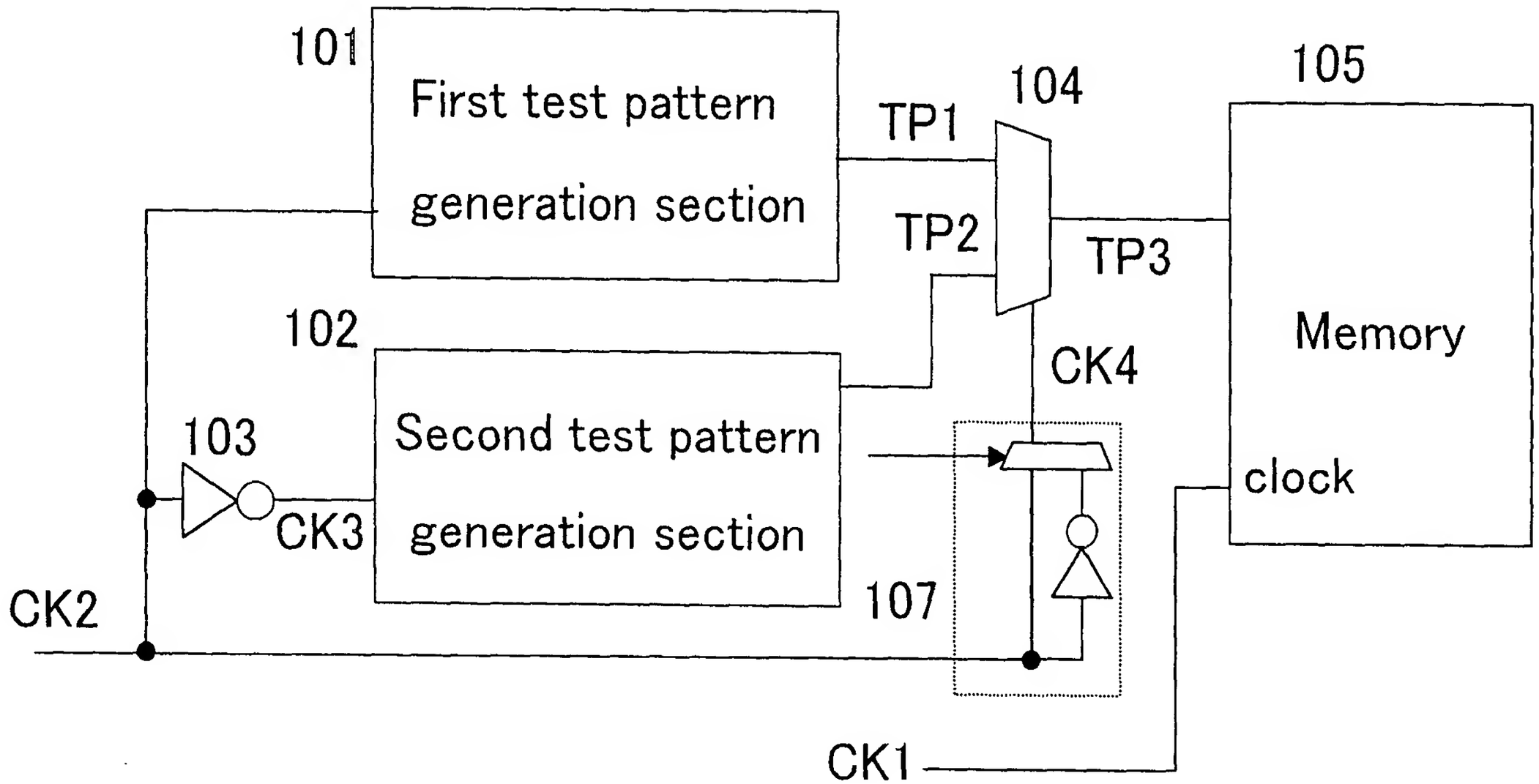
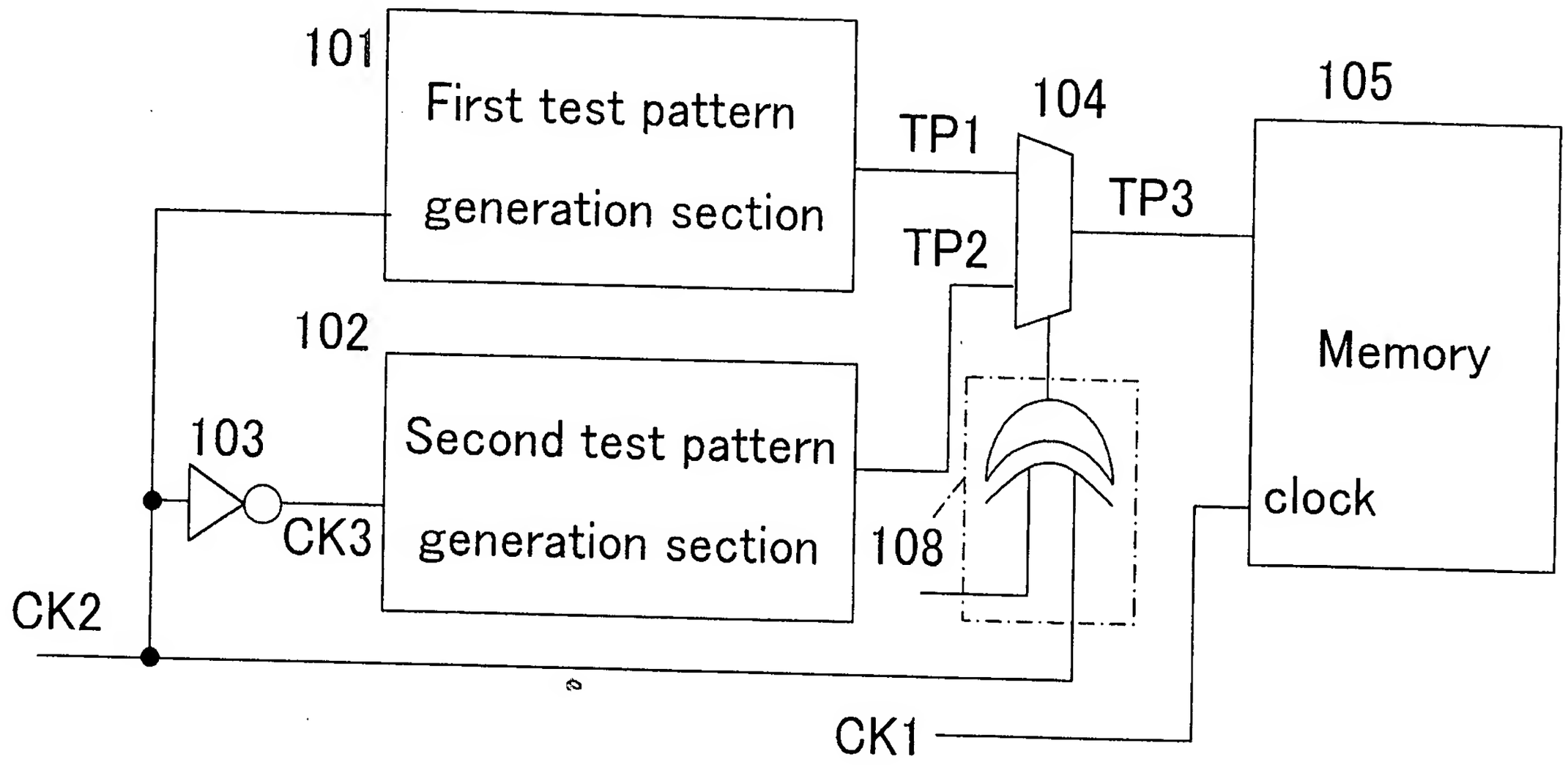

101
First test pattern generation section
TP1
104
105
TP2
TP3
Memory
clock
102
CK4
103
Second test pattern generation section
CK3
CK2
107
CK1

FIG. 27


101
First test pattern generation section
TP1
104
105
TP3
TP2
Memory
clock
102
103
Second test pattern generation section
CK3
108
CK2
CK1